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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,394	07/13/2001	Matthew D. Ornes	ZCOM.004US0	3741

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EXAMINER	
CHOU, ALBERT T	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/905,394	ORNES ET AL.	
	Examiner	Art Unit	
	Albert T. Chou	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8-12,18 and 25-27* is/are rejected.

7)☒ Claim(s) *2,4-7,13-17 and 19-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3, 8-12, 18 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Turner (US Patent Number: 5,339,311) hereinafter referred to as Turner.

Regarding claim 1, Turner teaches a data packet resequencer for a high speed data switch (Abstract; col. 1, lines 35-40; *an apparatus for reordering sequence indicated information units into proper sequence*) comprising:

- A **Resequencer Buffer 44**, controlled by a **Resequencing Buffer Controller 46**, (Figures 1 & 2; Abstract; col. 3, lines 38-41; *a double-back shifter*), receiving data packets from the high speed data **Switch 22** (Figures 1 & 2; Abstract; col. 1, lines 54-61; *receiving sequence indicated information units*); and
- A **Selection Circuit 45** (Figure 4; col. 4, line 2; *at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figure 4; col. 3, lines 65-68; *coupled to double-back shifter*), compares the age numbers and slot numbers to determine which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4;

to repetitively compare, reorder and shift said sequence indicated information units so as to be in proper sequence when shifted out of said double-back shifter).

Regarding claim 3, Turner teaches a **Selection Circuit 45** (Figure 4; col. 4, line 2; *at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figures 2 & 4; col. 3, lines 65-68; *sequence indicated information units stored in sets of corresponding storage units said double-back shifter*), compares the age numbers and slot numbers to determine which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4; *repetitively compares sequence indicators included in sequence indicated information units)*. The **Resequencer Buffer 44** and the **Resequencing Buffer Controller 46** then reorder the data packets for output in time sequence (Figure 2; col. 3, lines 52-56; *and reorders sequence indicated information units stored in associated storage units of said sets according to said comparisons*).

Regarding claim 8, Turner teaches high speed data switching systems, including **ATM switching systems** (Figure 1; col. 1, lines 16-17;*wherein said information units include sequence indicators for SONET payloads*), wherein switches have switching fabrics or other routing mechanisms, in conjunction with the **Resequencer Buffer 44** and the **Resequencing Buffer Controller 46,** for redirecting the flow of data packets from a plurality of inputs to a plurality of outputs (Col. 1, lines 16-20; *transmitted to a destination including said double- back shifter through a switch fabric from at least one Source*).

Regarding claim 9, Turner teaches high speed data switching systems, including **ATM switching systems** (Figure 1; col. 1, lines 16-17), wherein switches have switching fabrics or other routing mechanisms for redirecting the flow of data packets from a plurality of inputs to a plurality of outputs (Col. 1, lines 16-20; *wherein said at least one source, said destination and said switch fabric are a multi-shelf system*).

Regarding claim 10, Turner teaches a **Selection Circuit 45** (Figure 4; col. 4, line 2; *said at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figures 2 & 4; col. 3, lines 65-68), compares the age numbers and slot numbers to determine which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4; *compares in sequence indicated information units)*. The **Resequencer Buffer 44** and the **Resequencing Buffer Controller 46** then reorder the data packets for output in time sequence (Figure 2; col. 3, lines 52-56; *reorders sequence indicated information units having source indicators indicating a same source*). Regarding "*wherein said sequence indicated information units include source indicators indicating sources of received SONET payloads*" is inherent in Turner's invention since every ATM cell includes the VPI and VCI in the cell header.

Regarding claims 11-12, Turner teaches that data packets pass through a switching fabric along different paths (Col. 1, lines 21-25; *said plurality of switch slices form a distributed switch fabric)* in accordance with one of many methodologies designed to reliably route those data packets to their proper destination with minimal blocking (Col. 1, lines 21-25; *said switch fabric includes a plurality of switch slices)*.

Regarding claim 18, Turner teaches a method of using data packet resequencer for a high speed data switch (Abstract; col. 1, lines 35-40; *a method for reordering sequence indicated information units into proper sequence*) comprising:

- A step of using **Resequencer Buffer 44**, controlled by a **Resequencing Buffer Controller 46**, (Figures 1 & 2; Abstract; col. 3, lines 38-41; *a double-back shifter*), to receive data packets from the high speed data **Switch 22** (Figures 1 & 2; Abstract; col. 1, lines 54-61; *receiving sequence indicated information units*); and
- A step of using **Selection Circuit 45** (Figure 4; col. 4, line 2; *at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figure 4; col. 3, lines 65-68; *coupled to double-back shifter*), to compare the age numbers and slot numbers to determine which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4; *repetitively comparing, reordering and shifting said sequence indicated information units so as to be in proper sequence when shifted out of said double-back shifter*).

Regarding claim 25, Turner teaches high speed data switching systems, including **ATM switching systems** (Figure 1; col. 1, lines 16-17; *sequence indicated information unit of said SONET payloads*), wherein switches have switching fabrics or other routing mechanisms for redirecting the flow of data packets from a plurality of inputs to a plurality of outputs (Col. 1, lines 16-20; *receiving SONET payloads transmitted through a distributed switch fabric from a source*). Turner also teaches that

data packets from the Switch 22 are first accumulated in a **Resequencer Buffer 44** as controlled by a **Resequencing Buffer Controller 46** (Figure 2; col. 3, lines 38-41; *shifting at least one sequence indicated information unit of said SONET payloads into said double- back shifter upon each shift of said top row of said double- back shifter*).

Regarding claim 26, Turner teaches a method of using **Selection Circuit 45** (Figure 4; col. 4, line 2; *at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figures 2 & 4; col. 3, lines 65-68; *sequence indicated information units stored in sets of corresponding storage units said double-back shifter*), to compare the age numbers and slot numbers to determine which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4; *comparing)*. The **Resequencer Buffer 44** and the **Resequencing Buffer Controller 46,** each is associated with an I/O port (Figure 1; col. 1, lines 7-8; *source / destination port*), then reorder the data packets for output in time sequence (Figure 2; col. 3, lines 52-56; *and reordering sequence indicated information units having source indicators indicating a same source*).

Regarding claim 27, Turner teaches a method of using **Selection Circuit 45** (Figure 4; col. 4, line 2; *at least one circuit*), coupled to **Resequencer Buffer 44** and **Resequencing Buffer Controller 46** (Figures 2 & 4; col. 3, lines 65-68), to compare the age numbers and slot numbers to determine (Col. 4, lines 1-4; *comparing indicated information units having valid entry indicators indicating valid entries*) which data packet is the oldest and, hence, the next time in ordered sequence for transmission (Col. 4, lines 1-4; *reordering sequence indicated information units)*.

Allowable Subject Matter

3. Claims 2, 4-7, 13-17 and 19-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert T. Chou whose telephone number is 571-272-6045. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AC

Albert T. Chou

February 16, 2005

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